Multibit Data Storage States Formed in Plasma-Treated MoS_2 Transistors

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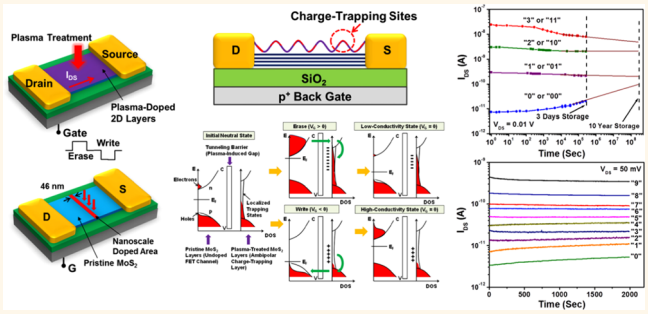
ABSTRACT New multibit memory devices are desirable for improving data storage density and computing speed. Here, we report that multilayer MoS_2 transistors, when treated with plasmas, can dramatically serve as low-cost, nonvolatile, highly durable memories with binary and multibit data storage capability. We have demonstrated binary and 2-bit/transistor (or 4-level) data states suitable for year-scale data storage applications as well as 3-bit/transistor (or 8-level) data states for day-scale data storage. This multibit memory capability is hypothesized to be attributed to plasma-induced doping and ripple of the top MoS_2 layers in a transistor, which could form an ambipolar charge-trapping layer interfacing the underlying MoS_2 channel. This structure could enable the nonvolatile retention of charged carriers as well as the reversible modulation of polarity and amount of the trapped charge, ultimately resulting in multilevel data states in memory transistors. Our Kelvin force microscopy results strongly support this hypothesis. In addition, our research suggests that the programming speed of such memories can be improved by using nanoscale-area plasma treatment. We anticipate that this work would provide important scientific insights for leveraging the unique structural property of atomically layered two-dimensional materials in nanoelectronic applications.



KEYWORDS: 2D layers · MoS_2 · transistor · memory · plasma etching · charge trapping

Although solid-state drives (SSDs) based on flash memory technology are extremely popular nowadays, they are still about 7 to 8 times more expensive per unit of storage than hard disk drives (HDDs). To produce much cheaper SSDs, it is desirable to develop new low-cost memory fabrication processes as well as new memory architectures for improving the storage density. One of such efforts is to create multibit data storage memory devices to achieve a higher storage density.[1−6] The fabrication of multibit (or multilevel cell (MLC)) flash memories needs precise deposition of multiple semiconductor layers and multiple overlay lithography processes to create complicated memory transistors consisting of multiple floating gates and blocking and tunneling layers.[1,2,7] This significantly increases the complexity of memory cells.[1,2,7] Although the state-of-the-art production lines for MLC flash memories are mature enough to enable low-cost manufacturing of such complicated cells, the future scale-down of MLC circuits beyond Moore's law will lead to the need for new MLC prototypes with much simpler architectures as well as new manufacturing systems with much lower processing cost and higher throughput. The recent efforts have demonstrated other prototype multibit memories based on different materials and device structures, including memories based on organic semiconductors with ambipolar transport properties,[3,8] memory transistors based on nanostructured materials,[4] flash memory-like transistors with capacitively coupled nanoparticle (NP)-based floating gates,[5] and multilevel resistive memories based on phase-change materials.[9] Relatively complicated and expensive processes are still demanded for making these devices. Therefore, it is always desirable to develop new multibit memories with a unique combination of excellent retention and endurance property, simple structure, and low fabrication cost.

Two-dimensional (2D) semiconducting layered transition metal dichalcogenides (LTMDs, *e.g.*, MoS_2, WSe_2, and WS_2) are envisioned as attractive materials for making new field-effect transistors (FETs) with a unique combination of excellent electronic

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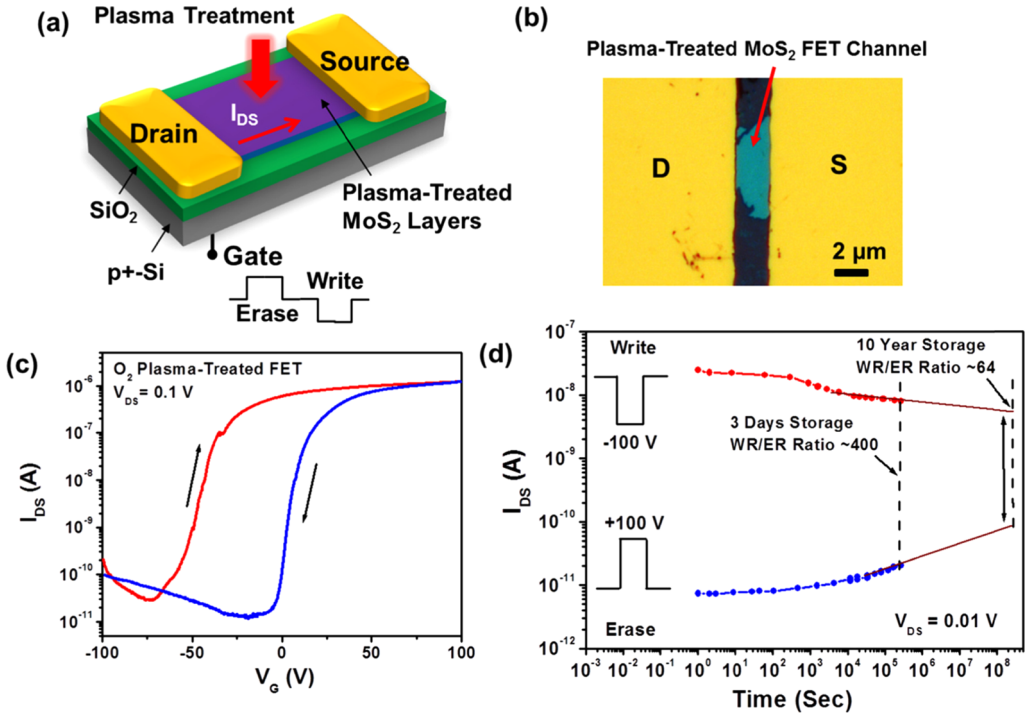

Figure 1. (a) Illustration of a back-gated MoS_2 memory FET created by a simple plasma treatment. (b) Optical micrograph of a memory FET consisting of an O_2 plasma-treated MoS_2 channel (thickness: 20 nm, length: 2 μm, average width: ~5 μm), Ti/Au D/S contacts, and a p^+-Si back gate. (c) Transfer curves ($I_{DS}-V_G$ curves acquired along two different V_G sweep directions with a sweep rate of 10 V/s) and (d) retention characteristics ($I_{DS}-t$ curves under V_{DS} = 0.01 V and V_G = 0 V recorded for 3 days) of the memory FET shown in (b). The insets in (d) show the ±100 V, 1 s V_G pulses applied at the back gate for retention measurements. The WR/ER ratio after 3 days is measured to be ~400. The WR/ER ratio after 10 years is estimated to be ~64, which is suitable for long-term binary data storage.

and mechanical properties, low manufacturing cost, and potential large-area integration capability.[10−24] Especially, the stacking of MoS_2 layers and other 2D layers has been used for making new high-performance nonvolatile memory transistors.[25−29] These works have motivated and inspired additional research efforts to leverage unique electronic and structural properties of emerging 2D materials for making new material- and cost-efficient memory devices.

In this article, we present the fabrication and characterization of new MoS_2-based floating-gate-free, nonvolatile, multibit memory FETs with excellent retention and endurance properties as well as extremely simple structures. These multibit memory FETs were dramatically created by treating MoS_2 FET channels with highly energetic plasmas. Using such plasma-treated MoS_2 FETs, we have demonstrated highly reliable binary and 2-bit (*i.e.*, 4-level) data states with potential for year-scale data retention, as well as 3-bit (*i.e.*, 8-level) data states suitable for at least day-scale storage. In addition, our research shows that the memory FETs fabricated by nanoscale-area plasma treatment exhibit a faster programming speed than the FETs made by blank plasma treatment. Such a new memory capability is hypothesized to be caused by the spontaneous separation of plasma-doped MoS_2 layers from undoped layers, which could form an ambipolar charge-trapping layer interfacing the FET channel through a tunneling barrier. This structure could enable the nonvolatile retention of charged carriers as well as the reversible modulation of polarity and amount of the trapped charge, therefore resulting in multilevel data states in FETs. Our Kelvin force microscopy results strongly support this hypothesis. This work may leverage the unique structural property of 2D materials for applications in the fields related to data storage technologies. The presented fabrication methods and device structures hold a significant potential to be further developed into a low-cost, upscalable memory solution for making future high-performance disposable electronic products such as electronic labels, digital newspapers, medical care tags, and point-of-care biosensors. In addition, the presented multibit memory solution based on simple plasma doping processes could fulfill the predictable needs associated with the future scale-down of MLC circuits very well because of its unique simplicity and compatibility with already established manufacturing facilities.

RESULTS AND DISCUSSION

Figure 1a illustrates the conversion of a MoS_2-based back-gated FET into a memory FET through treating the top surface of the MoS_2 channel with energetic plasmas (*i.e.*, CHF_3-, CF_4-, and O_2-based plasmas

generated in a reactive ion etcher (RIE)). The details about the initial FET fabrication and the plasma treatment are described in the Methods and Materials section. Figure 1b shows the optical micrograph (OM) of an exemplary MoS_2 memory FET treated with O_2 plasma (channel length: $L = 2\ \mu m$; channel width: $W \approx 5\ \mu m$; MoS_2 thickness: $t_{MoS2} \approx 20$ nm). The fabricated memory FETs are characterized following the measurement processes described in the Methods and Materials section.

First, we measured the transfer characteristics (*i.e.*, drain−source current (I_{DS})−gate voltage (V_G) curves acquired along two different V_G sweep directions with a sweep rate of 10 V/s under a fixed drain−source voltage (V_{DS})) of an untreated pristine MoS_2 FET that exhibits a mild hysteresis, as shown in Figure S1 (see the Supporting Information). This mild hysteresis was attributed to the charging and discharging processes associated with the charge-trapping sites at the MoS_2/SiO_2 interface.[30] As indicated by the previous work, such charge-trapping sites can retain the trapped charge for relatively short time durations (trapping time constants (τ) range from 30 to 500 s),[30] not suitable for data storage applications. We subsequently measured the transfer characteristics of a MoS_2 FET treated with water vapor by using an atomic layer deposition (ALD) tool (see the Supporting Information for details of this treatment process). As shown in Figure S2a, this moisture-treated FET exhibits a much more prominent $I_{DS}-V_G$ hysteresis as compared to the untreated FET. Such a large hysteresis was attributed to the high density of moisture-induced charge traps, and it motivated us to characterize the retention properties (*i.e.*, $I_{DS}-t$ characteristics acquired under fixed V_{DS} and V_G after the initial settings of the FET with specific V_G pulses) of the trapped charge (or potential binary memory states) in this moisture-treated FET. Figure S2b shows $I_{DS}-t$ curves of potential "write (WR)" and "erase (ER)" data states of this moisture-treated FET, which were configured by the application of ±100 V, 1 s V_G pulses. After the initial device settings, the I_{DS} values of so-called "write" and "erase" states quickly relaxed to almost the same value after ~1000 s. This test indicates that although the water molecules adsorbed on MoS_2 FETs can induce a prominent hysteresis of transfer curves, the charge-trapping times of such FETs are too short to enable long-term data storage.

In contrast to untreated and moisture-treated MoS_2 FETs, all plasma-treated FETs exhibit well-differentiated binary data states with excellent retention properties. For example, Figure 1c and d display transfer and retention characteristics of an O_2 plasma-treated FET (*i.e.*, the one shown in Figure 1b), respectively. This memory FET exhibits a high WR/ER ratio (*i.e.*, $I_{DS(WR)}/I_{DS(ER)}$) that was measured to be $\sim 10^3$ after a 1 h retention test and ~400 after a 3-day retention test. Based on the 3-day retention test data plotted in Figure 1d, the WR/ER ratio after 10 years is estimated to be ~64, which can still enable an unambiguous reading of distinguishable I_{DS} values for "write" and "erase" states. Figure S3 in the Supporting Information shows the transfer and retention characteristics of exemplary CF_4 and CHF_3 plasma-treated MoS_2 memory FETs. CF_4 and CHF_3 plasma-treated FETs typically exhibit relatively lower WR/ER ratios (10 to 100 after 2000 s retention tests) in comparison with those of O_2 plasma-treated ones (100 to 1500 after 2000 s retention tests). These characterizations show that plasma-induced (especially, O_2 plasma-induced) charge-trapping levels in MoS_2, in comparison with the traps at MoS_2/SiO_2 interfaces and moisture-induced traps, can retain trapped charges for a much longer time and are potentially suitable for long-term data storage applications. In addition, the areal density of such plasma-induced charge-trapping states can be estimated by using $\sigma_N = C_{ox}\Delta V_G/2e$, where ΔV_G is the hysteresis window, C_{ox} is the gate dielectric capacitance, and e is the elementary charge.[26] As shown in Figure 1c, ΔV_G is about 50 V and σ_N is estimated to be $\sim 10^{12}$ cm^{-2}.

O_2 plasma-treated FETs were further used for demonstrating multibit storage capability. To obtain an n-bit/FET storage capability, a memory FET needs to have at least 2^n distinguishable data levels. For example, the same FET shown in Figure 1d was used for realizing 2-bit storage that needs 4 data levels. Figure 2a sketches four V_G signals used for configuring this memory FET into 4 data states ("00", "01", "10", "11"). Here, the signals labeled with "00" and "11" are exactly the same ± 100 V, 1 s V_G pulse signals used for setting the FET into binary "erase" (now as "00") and "write" (now as "11") states, respectively. The V_G signal for setting the "01" ("10") state is a dual-pulse signal that consists of one −100 V (+100 V), 1s pulse (V_{G1}) immediately followed by another +75 V (−75 V), 1 s pulse (V_{G2}). Here, the first pulse (V_{G1}) is used to release any previously trapped charge that has the same polarity as that of the to-be-refreshed charge or reset the FET back to the initial neutral state. The second pulse (V_{G2}) sets the FET with a new charging state. Figure 2b shows the 3-day retention test data of 4 data levels. On the basis of the extrapolated $I_{DS}-t$ curves (solid lines in log scales) shown in Figure 2b, these 4 data states are anticipated to be still distinguishable after 10 years. Therefore, this O_2 plasma-treated MoS_2 FET can serve as a 2-bit memory with a year-scale data storage capability.

Another O_2 plasma-treated FET was set into 10 distinguishable data states ("0" to "9") by using the dual-pulse V_G signals sketched in Figure 2c. The second pulses (V_{G2}) of these signals have different polarities and amplitudes, which can result in different amounts and polarities of the trapped charge in the FET and therefore generate multiple data levels. Figure 2d shows the retention behaviors of these 10 data levels. On the basis of the retention test data, it is estimated

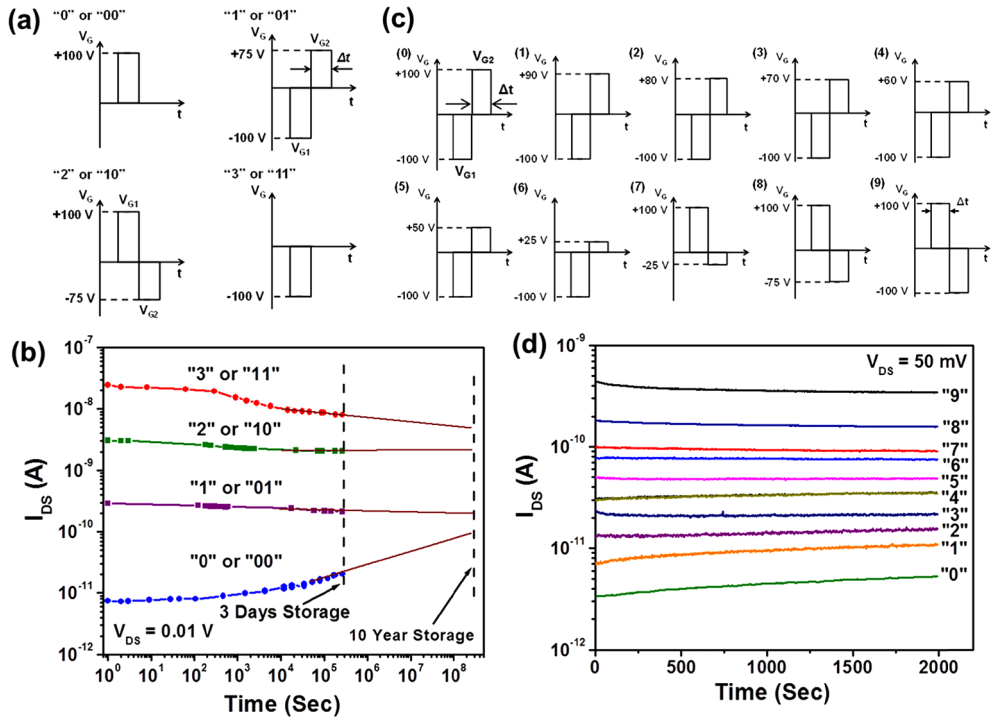

Figure 2. (a) V_G signals used for programming the memory FET (the one shown in Figure 1) into 4 data states ("00", "01", "10", "11", *i.e.*, a 2-bit memory). (b) Retention characteristics of 4 data states recorded for 3 days. For these retention measurements, V_{DS} = 0.01 V, V_G = 0 V. It is estimated that these 4 data states can be well discernible within 10 years of the initial applications of programming V_G signals. (c) V_G signals for programming another plasma-treated MoS_2 memory FET into 10 data states. (d) Retention characteristics of 10 well-discernible data states recorded for 2000 s. For these 10 retention measurements, V_{DS} = 0.05 V, V_G = 0 V.

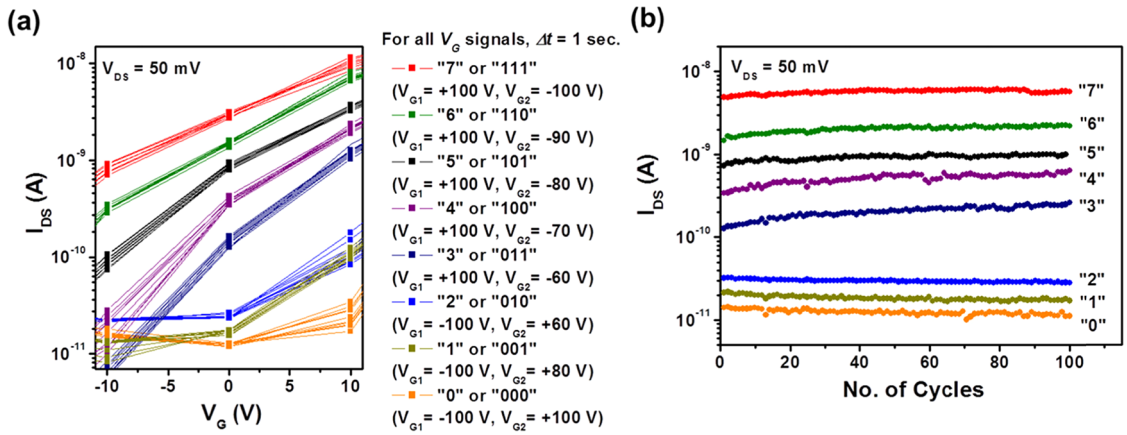

Figure 3. Switching endurance characteristics of a MoS_2 memory FET: (a) Transfer curves (I_{DS}–V_G curves) corresponding to 8 data states measured for 10 sequential cycles; (b) data levels (I_{DS} values measured at V_{DS} = 0.05 V, V_G = 0 V after the applications of programming V_G signals) recorded for 100 sequential cycles (for each endurance characterization cycle, the memory FET is sequentially programmed into "000" to "111" states, demonstrating a repeatable 3-bit memory capability).

that these 10 data levels are distinguishable within day-scale time durations after the initial setting (see Figure S4). Therefore, such a memory FET can enable a 3-bit (at least 8 data levels) storage capability and can be used for electronic applications requiring hour- or day-scale data storage functionalities, such as central processing unit (CPU) cache memories, disposable electronic tags, and buffer memories for displays.

To evaluate the endurance property of multibit memory states, an O_2 plasma-treated FET was periodically programmed into 8 data states (*i.e.*, "0" to "1" to "2" ... to "7", then repeat) by repeatedly applying 8 dual-pulse V_G signals, as indicated in Figure 3a. When the FET was switched into a data state, its current transfer characteristic curve (*i.e.*, I_{DS}–V_G curve for V_G = −10 to 10 V; V_{DS} = 50 mV) was recorded. Figure 3a shows the transfer curves corresponding to 8 data states that were recorded during the first 10 programming cycles. Figure 3b plots I_{DS} values (measured under V_G = 0 V, V_{DS} = 50 mV) of 8 data states recorded

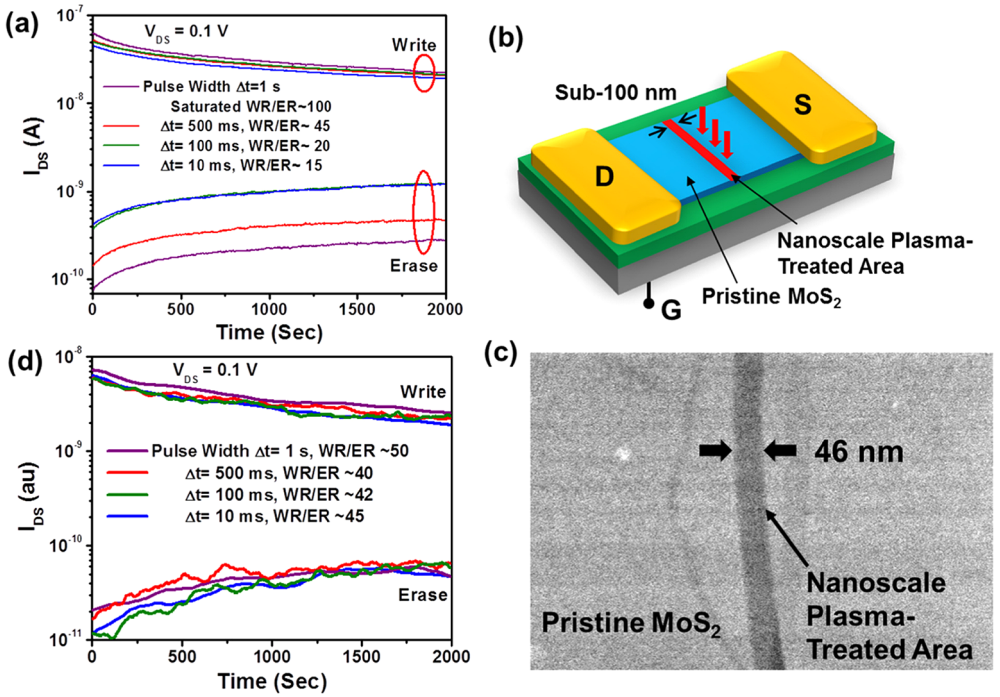

Figure 4. (a) Retention characteristics of the binary data states in a microscale size memory FET (channel length: 2 μm, width: ~5 μm), which were measured after the device was programmed by ±100V V_G pulses with different pulse durations (Δt = 10 ms, 100 ms, 500 ms, and 1 s). (b) Illustration of a MoS_2 memory FET fabricated by using selected-area plasma treatment. Here, the plasma-treated region is a sub-100 nm wide nanoline across the whole MoS_2 channel. (c) SEM image of a 46 nm wide plasma-treated line region across a pristine MoS_2 FET channel that was formed by using O_2 plasma treatment through an EBL-patterned PMMA resist layer. (d) Retention characteristics of the binary data states in the MoS_2 memory FET shown in (c), which were measured after the device was programmed by ±100V V_G pulses with different pulse durations.

for 100 cycles. These results indicate that plasma-induced multibit memory states exhibit a good endurance property.

To evaluate the effect of the V_G pulse duration (Δt) on the resulting data levels, we measured the retention curves of the binary data levels of an O_2 plasma-treated FET ($L \approx 2$ μm, $W \approx 5$ μm) after it was set by applying ±100 V V_G pulses with different time durations ranging from 10 ms to 1 s (Figure 4a). Figure 4a shows that the I_{DS} value of the "write" state exhibits a weak dependence on Δt, whereas the I_{DS} value of the "erase" state highly depends on Δt, therefore resulting in a strong dependence of the WR/ER ratio on Δt. When Δt is reduced from 1 s to 10 ms, the WR/ER ratio drops from ~100 to 15. This suggests that a long pulse duration ($\Delta t > 1$ s) may be needed to fully charge (or discharge) all plasma-induced charge-trapping states in a microscale size FET. Assuming that the capacitance associated with plasma-induced charge-trapping states is proportional to the total MoS_2 surface area treated with plasma, the required memory setting time is anticipated to be scaled down with reduction of the total plasma-treated area (*e.g.*, using the selected-area plasma treatment). Figure 4b illustrates a MoS_2 memory FET with a selected area treated with plasma. Here, the selected area is a line with a nanoscale width across the whole FET channel. Figure 4c shows a zoomed (in-lens mode) scanning electron microscope (SEM) image of a MoS_2 FET surface with a 46 nm wide plasma-treated line region across the whole FET channel, which was formed by using O_2 plasma treatment through a PMMA resist layer patterned by electron-beam lithography (EBL). Figure 4d displays the retention curves of binary data levels of this memory FET after it was set by applying ±100V V_G pulses with different time durations ranging from 10 ms to 1 s. Although this FET has the same total channel area (*i.e.*, $L \approx 2$ μm, $W \approx 5$ μm) as that of the blank-treated FET shown in Figure 4a, both its "write" and "erase" I_{DS} values as well as WR/ER ratio exhibit a quite weak dependence on Δt values. This indicates that the selected-area plasma treatment, as compared to the blank treatment, can result in a much smaller capacitance of plasma-induced charge-trapping states and therefore a faster memory setting speed, but can still generate reasonably good WR/ER ratios (40 to 100) suitable for practical memory-related applications. The result shown in Figure 4 also implies that our MoS_2 memory FETs could be scaled down to the smaller devices with sub-50 nm scale channel lengths. Such sub-50 nm size memory FETs are also anticipated to have faster writing/erasing speeds as compared to the current microscale ones.

To explore the physical mechanism responsible for the observed memory capability, we captured SEM images of MoS_2 surfaces treated with O_2 plasma. The SEM image in Figure 5a shows that the O_2 plasma-treated MoS_2

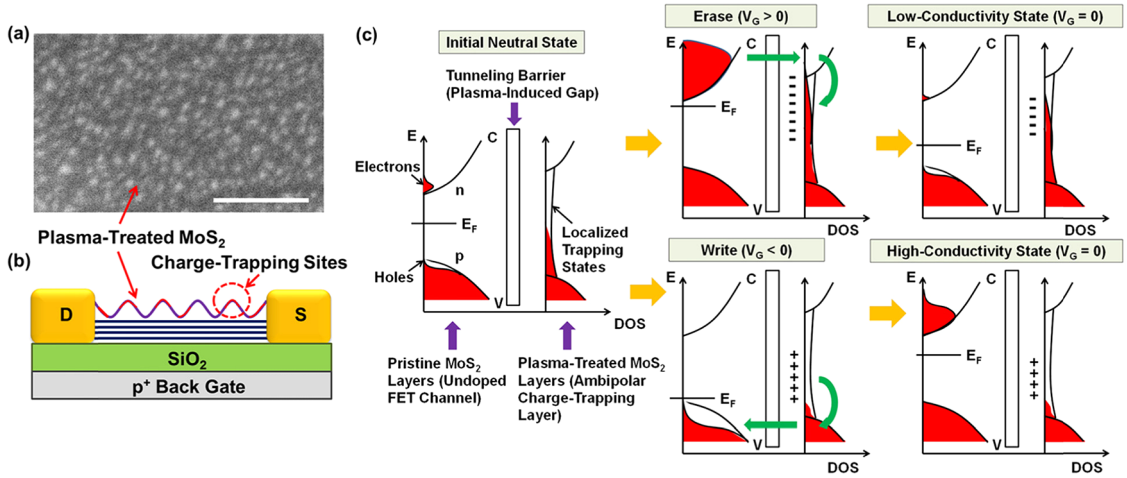

Figure 5. (a) SEM image of an O_2 plasma-treated MoS_2 surface that features nanoscale roughness features (the scale bar is 100 nm). (b) Cross-sectional illustration of a MoS_2 memory FET treated with plasma. The top few MoS_2 layers become rough because of the doping of plasma species. Part of the treated layers may be mechanically separated and electrically insulated from the intact underlying layers and, therefore, can serve as a nonvolatile charge-trapping layer. The plasma-induced gap between this charge-trapping layer and the intact MoS_2 channel can serve as a tunneling barrier layer. (c) Hypothesized write/erase schemes of plasma-treated MoS_2 memory FETs.

surface exhibits a nanoscale roughness with average period of ~10 nm. Such a roughness, in contrast with the flat surface of a pristine MoS_2 sample, is attributed to the plasma-induced doping of external atoms, which can induce an expansion of the MoS_2 layers and let these layers ripple up and down.[31] This ripple effect could partially exfoliate the plasma-doped top layers from the undoped pristine MoS_2 layers and form charge-trapping sites slightly isolated from the FET channel, as illustrated in Figure 5b. The gap size between such charge-trapping sites and the undoped MoS_2 channel is estimated to be on the same order of magnitude as the average period of the ripple features in the top layers (*i.e.*, 5−10 nm). This gap may serve as a tunneling/blocking barrier layer for retaining trapped charges and switching the memory states. On the basis of this analysis, we have hypothesized a possible write/erase mechanism to preliminarily explain the memory capability of plasma-treated MoS_2 FETs. Figure 5c illustrates the hypothesized band structure (*i.e.*, the density of states (DOS) function) of a plasma-treated MoS_2 FET. The untreated (or pristine) MoS_2 layers (*i.e.*, the FET channel region) are expected to have a typical band structure of lightly doped semiconductors with a relatively low density of impurity states in the band gap, whereas the plasma-treated top layers are expected to exhibit many plasma-induced localized trapping states in the band gap. It is also assumed that these trapping states could be distributed over a broad energy range in the band gap, and they are likely to be a mixture of donor-type, acceptor-type, and isoelectronic deep-level traps. Such a large variety and broad energy distribution of plasma-induced traps are hypothesized based on the fact that energetic plasma species, similar to electron irradiation, could generate a broad variety of defect configurations in MoS_2 layers, including sulfur vacancies, substitutional donor/acceptor defects, adatoms with charge, and isoelectronic impurities.[14,31−33] Therefore, the plasma-treated MoS_2 top layers may serve as an ambipolar charge-trapping layer. At the initial neutral state, the net charge in the plasma-treated layers is assumed to be close to zero (*i.e.*, all donor-type traps are occupied with electrons, and all acceptor-type traps are vacant). To obtain an "erase" ("write") state, a positive (negative) V_G pulse is applied. In this case, the Fermi level is elevated (lowered) and the conduction (C) (valence (V)) band of untreated layers (*i.e.*, the FET channel) is populated with electrons (holes). These electrons (holes) have a high probability to tunnel through the barrier and are injected into the conduction (valence) band of the plasma-treated top layers. The injected electrons (holes) may quickly relax to the localized trapping states with lower energies. When the V_G is set back to zero, the trapped electrons (holes) could be retained in the top layers for a long storage time, because of the existence of a barrier layer between plasma-treated and untreated layers as well as the lack of target states in the band gap of untreated layers that can effectively prevent electrons (holes) from tunneling back from the trapping states to the FET channel. This model also implies that the V_G pulse amplitude could modulate the total amount of charged carriers injected into the charge-trapping states in plasma-treated MoS_2 layers. Such trapping states, very likely different from the discrete trap levels in conventional memory FETs with floating gates, may be distributed over a broad energy range and could accommodate different amounts of injected carriers with different polarities, therefore resulting in multiple data levels (*i.e.*, multiple I_{DS} values). Such a hypothesized model could preliminarily explain the observed multibit data storage capability. In addition, as implied by this model, the electrons (holes) trapped at relatively high energy states that are close to the

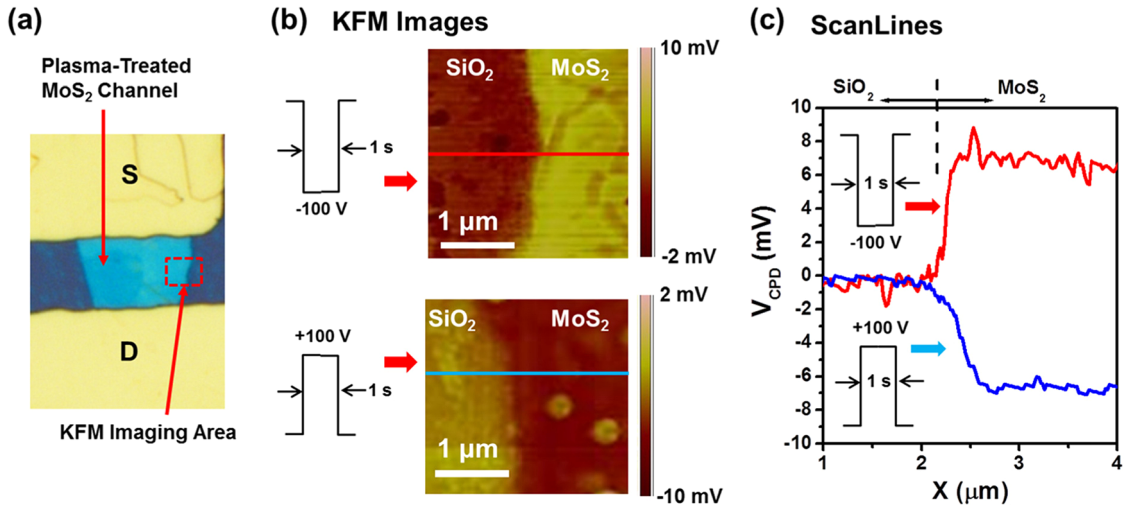

Figure 6. (a) Optical image of a plasma-treated MoS_2 memory FET used for KFM imaging. The dashed box indicates the KFM imaging region. (b) KFM images of the MoS_2 channel captured after the FET was programmed by −100 V, 1 s (top) and +100 V, 1 s (bottom)V_G pulses, respectively. (c) KFM scanlines showing the V_{CPD} values of the MoS_2 channel after the FET was programmed by −100 V, 1 s (red line) and +100 V, 1 s (blue line) V_G pulses, respectively.

conduction (valence) band could easily tunnel back to the FET channel and result in a slow relaxation of I_{DS} values with time. During the initial memory setting, the higher V_G pulse could induce the trapping of more charged carriers in such high-energy states and therefore result in a more prominent relaxation of I_{DS} values with time. This implication from the model is consistent with our observation in the retention tests (*e.g.*, see Figure 2b and d) that the data states with the highest or the lowest I_{DS} values, typically configured by ± 100 V V_G pulses, exhibit more prominent relaxation behaviors than other intermediate data states between them.

To further support our model and verify that plasma-treated MoS_2 layers can indeed serve as charge-trapping layers, we used a Kelvin force microscope (KFM) to image and measure the contact potential (or work function) difference (V_{CPD}) between V_G-modulated MoS_2 FET surfaces and the KFM tip. Figure 6a shows the OM of an O_2 plasma-treated MoS_2 FET, in which the dashed box denotes the KFM-imaged area. Figure 6b displays two KFM images that were captured after the FET was configured by applying a −100 V, 1 s V_G pulse and a +100 V, 1 s V_G pulse, respectively. The scanlines denoted by the solid lines are accordingly plotted in Figure 6c. Figure 6b and c explicitly show that the polarity switching of the applied V_G pulse can accordingly switch the V_{CPD} polarity on the MoS_2 surface but does not noticeably change the V_{CPD} value on the SiO_2 surface. Here, the V_{CPD} value on the MoS_2 surface is directly associated with the electrostatic interaction between the trapped charge in the top MoS_2 layers and the KFM tip.[34,35] It should be noted that the charge trapped at other interfaces (*e.g.*, MoS_2/SiO_2 and Si/SiO_2 interfaces) can hardly affect the V_{CPD} value on the MoS_2 surface because of the screening effect of multilayer MoS_2 channels (the electric-field screening length in MoS_2 is 3−5 nm; the thickness of our FET channels is 20−30 nm).[35] Therefore, it is concluded that the V_G-modulated memory states observed in our MoS_2 FETs are attributed to the charge-trapping states in plasma-treated top MoS_2 layers, which can enable the ambipolar charge retention and modulation. This conclusion is also consistent with our hypothesized model. Here, although the electric field generated by the back gate is expected not to directly affect the charge-trapping states in the plasma-treated top layers,[35] this gating field can directly modulate the carrier (electron or hole) concentrations in the untreated layers, and these densely populated carriers could diffuse to the interface between untreated and treated layers and subsequently transport through the tunneling barrier formed at this interface, as illustrated in Figure 5c. In this way, the back gate voltage could indirectly modulate the charge trapping and switching in the top MoS_2 layers. Future research will use high-resolution microscopes (*e.g.*, high-resolution transmission electron microscopes (HRTEMs)) to directly image the atomic morphology of plasma-induced charge-trapping sites in MoS_2 layers, which is anticipated to provide more precise scientific insights for understanding the observed multibit memory capability.

Finally, we discuss the uniformity issue of our MoS_2 memory FETs. Although it is possible to create reliable individual memory FETs and observe durable multibit memory states in our experiments, our current FETs still exhibit prominent device-to-device variations in WR/ER ratios (*i.e.*, the absolute dynamic range of I_{DS} values for possible memory states), I_{DS} values for specific memory states (or data levels), and on/off ratios of initial FETs. Such variations are attributed to our current poor control of the geometry parameters of MoS_2 channels (*i.e.*, width, length, and thickness

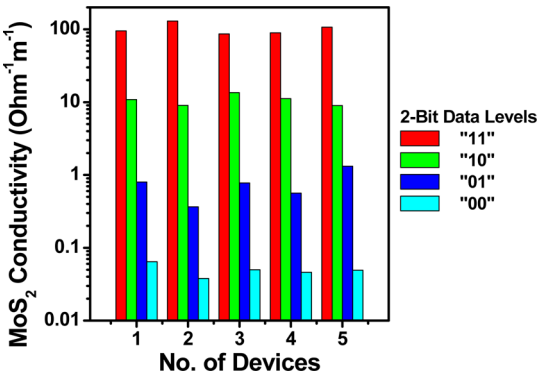

Figure 7. Two-bit data levels (*i.e.*, "00", "01", "10", "11" states) of five O_2 plasma-treated MoS_2 memory FETs fabricated in the same batch. Note that here the data levels are denoted by the conductivity of MoS_2 FET channels instead of I_{DS} values, which exhibit a reasonably good device-to-device uniformity and consistence.

parameters of MoS_2 FET channels) and the fabrication-introduced unexpected impurities. In particular, different lateral pattern shapes of MoS_2 channels can result in different channel conductance (or I_{DS}) values, different MoS_2 thicknesses can result in different on/off and WR/ER ratios, and unexpected impurities introduced by the fabrication processes could modify the DOS profile of charge-trapping states in plasma-treated MoS_2 layers, resulting in an observable variation in the ratios of I_{DS} values for multiple data levels. These technical issues need to be addressed to ultimately enable the implementation of our MoS_2 memory FETs into large-area memory cell array architectures. On the basis of current rapid development of 2D-layer technologies, these problems are anticipated to be solved in the near future through developing new nanomanufacturing processes capable of producing highly uniform MoS_2 FET array patterns with well-controlled doping profiles.

To further justify this anticipation, we characterized five memory FETs that were fabricated in the same batch and were expected to have very similar doping profiles in their MoS_2 channels. All five devices have very close MoS_2 channel thicknesses (20 to 25 nm) and lengths (~5 μm), but very different channel widths (2−10 μm). To eliminate the effect of lateral pattern shapes on the memory data levels, we used the average conductivity (σ) values, instead of I_{DS} values, of MoS_2 channels to denote the memory states. Figure 7 plots the 2-bit data levels of these five memory FETs, which were measured after the FETs were set by the V_G signals listed in Figure 2a. Here, these FETs exhibit a reasonably good uniformity and consistency in all plasma-induced data levels. This result implies that through carefully unifying the processing conditions and device geometries, it is highly possible to make large arrays of plasma-treated MoS_2 memory FETs with a high uniformity at all registered data levels.

CONCLUSION

In conclusion, we dramatically found that the plasma-treated MoS_2 FETs can serve as multibit memory devices with a year-scale 2-bit/transistor (or day-scale 3-bit/transistor) storage capability. SEM and KFM characterization results suggest that such a data storage capability could be attributed to the plasma-induced ripple and partial separation of the top MoS_2 layers from the underlying pristine layers, which could spontaneously form a memory FET structure bearing an ambipolar charge-trapping layer coupled with the FET channel through a tunneling barrier. Such multibit memories exhibit a unique combination of excellent retention and endurance characteristics, extremely simple structures, and low fabrication costs. Our work also shows that the programming speed of such memories can be further improved by using nanoscale-area plasma treatment processes. We anticipate that this work would greatly leverage the unique structural property of MoS_2 and other emerging 2D layered materials for nanoelectronic applications. The presented fabrication methods and device structures hold a significant potential to be further developed into a low cost, upscalable memory solution for making future high-performance disposable electronic products. Especially, our plasma-treated MoS_2 memory FETs with no need of complicated floating-gate structures could be easily scaled down and exhibit a significantly improved writing speed as compared to current MLC memories.

METHODS AND MATERIALS

Fabrication of the Initial Field-Effect Transistors Using Exfoliated Pristine MoS_2 Flakes. In this work, the initial MoS_2 FETs are fabricated by using a printing-based approach previously published.[15] MoS_2 channel thicknesses (t_{MoS2}) are specifically controlled to be 15−30 nm, aiming to achieve relatively high field-effect mobility values (μ = 20 to 30 cm^2/Vs).[31,36] The channel lengths (L) are 2 to 10 μm, and the average channel widths (W) are 5 to 15 μm. Ti (5 nm)/Au (50 nm) electrode pairs serve as drain (D) and source (S) contacts, which are fabricated by using photolithography followed by metal deposition and lift-off in a solvent. The p^+-Si substrates are used as back gates (G). Thermally grown SiO_2 layers (300 nm thick) are used as the gate dielectrics. Here, the reason that such relatively thick SiO_2 layers are used as gate dielectrics is that we employ a simple color coding method for quickly locating MoS_2 flakes with suitable thicknesses (15−30 nm).[37] In this method, MoS_2 flakes are usually deposited on Si substrates coated with 300 nm thick SiO_2 layers, which can result in an optimal color contrast of few-layer MoS_2 device features against the substrate background under the illumination of a regular photoaligner and can therefore make it convenient to perform overlay alignment. However, using other more advanced tools for imaging MoS_2 features (*e.g.*, a Micro-Raman tool), 300 nm thick gate dielectrics may not be a must here, and our memory FETs could be made on much thinner gate dielectrics to scale down the required programming voltages.

Plasma Treatment for Converting MoS_2 FETs into Multibit Memory FETs. The top surface layers of MoS_2 FET channels are treated (or doped) with various plasmas (*i.e.*, O_2, SF_6, CF_4, and CHF_3) in an inductively coupled plasma-based reactive ion etching tool. For all plasma recipes, the RF power is fixed to 200 W, the pressure is 10 mTorr, the precursor gas flow rate is 10 sccm, and the treatment time for each FET is fixed to 2 min. The surface morphology of plasma-treated MoS_2 FETs is characterized by using a scanning electron microscope.

Electronic Characterizations of Plasma-Induced Binary and Multibit Memory States. The memory FETs are characterized by using a HP4145 semiconductor parameter analyzer that can generate gate voltage (V_G) pulses with duration widths ranging from 10 ms to 1 s. To characterize the hysteretic behaviors of the transfer curves of memory FETs, drain−source current (I_{DS})−gate voltage (V_G) curves are acquired along two different V_G sweep directions with a constant sweep rate of 10 V/s. To configure a memory FET into binary data states, a +100 V (−100 V) V_G pulse (duration Δt: 10 ms to 1 s) is applied to induce a low (high)-conductance "erase" ("write") state in the FET. To evaluate the retention properties of data states, time-dependent I_{DS} values (*i.e.*, $I_{DS}-t$ curves) are measured under fixed V_{DS} and V_G (typically V_G = 0 and V_{DS} = 0.01 to 0.1 V) after the initial settings of the memory FET with specific V_G pulses. A Kelvin force microscope (Veeco NanoMan Dimension V system equipped with Pt/Ir-coated tips with tip radius $R \approx 20$ nm and resonant frequency $f_0 \approx 75$ kHz) is employed to probe the polarity and amount of the trapped charge in plasma-treated MoS_2 layers, which are modulated by the V_G pulse amplitude.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Transfer curves of an untreated pristine MoS_2 FET (Figure S1); treatment of MoS_2 FETs with water vapor (moisture) by using atomic layer deposition processes; transfer and retention characteristics of a MoS_2 FET treated with moisture (Figure S2); transfer and retention characteristics of FETs treated with CF_4 and CHF_3 plasma recipes (Figure S3); retention characteristics of 10 data states of an O_2 plasma-treated MoS_2 FET (Figure S4). This material is available free of charge *via* the Internet at http://pubs.acs.org.

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